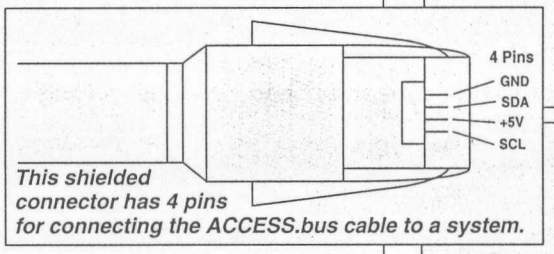
Special Report: ACCESS.bus Specs And Products

The development of ACCESS.bus, a communications protocol for connecting multiple, low-speed I/O devices to a single computer port, and the formation last June of the ACCESS.bus Industry Group (ABIG) is spawning creation of a rapidly growing number of hardware and software products based on the ACCESS.bus' connectivity specs (see chart below). ACCESS.bus was jointly developed by Digital Equipment Corp. and Philips Semiconductors and is now owned and supported by ABIG, who is promoting the new bus as an industry standard. To date, up to 125 peripheral devices, including keyboards, mice, scanners, digitizers, and bar code readers have been made to operate independently on a single computer port.

At the hardware level, ACCESS.bus uses the I²C (Inter-Integrated Circuit) serial bus developed by Philips several years ago to simplify automotive electronics and other distributed control systems. This serial bus is designed to carry 1 bit of information at a time on a single data line. Today, a host of low-cost I²C components are readily available to handle the logical complications associated with bit-level handshaking.



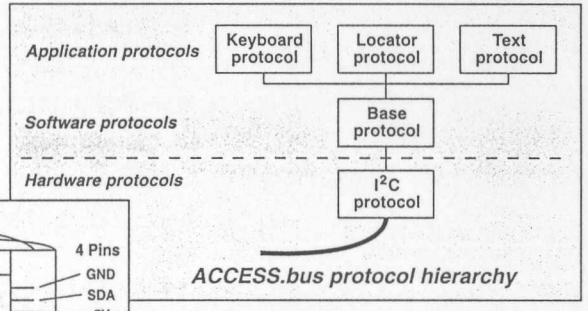
This shielded connector has 4 pins for connecting the ACCESS.bus cable to a system.

The physical medium for ACCESS.bus is a shielded cable with four wires for handling serial data (SDA), serial clock (SCL), power (5V), and ground (GND). The SDA and SCL lines work together to define information carried on the bus, and the host computer drives the 5V power line with a minimum of 50 mA to supply peripheral devices (peripherals can also be externally powered). A typical ACCESS.bus device has two connectors, permitting two or more peripherals to be daisy-chained together on the bus (handheld devices can have a captive cable joined to the bus trunk with a T-connector).

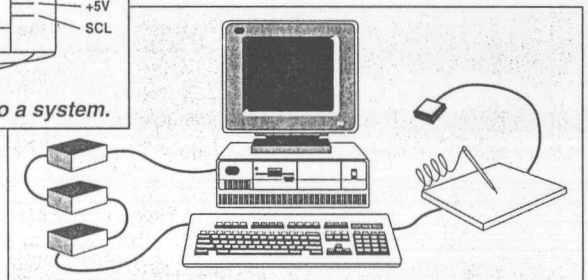
I²C technology supports clock rates up to 100 kHz and the maximum ACCESS.bus data transfer rate is approximately 80 kbits/s.

The ACCESS.bus communications protocol has three layers: I²C, Base and Applications. The I²C Protocol defines a symmetric, multi-master bus on which arbitration among contending masters is effected without losing data. I²C provides cooperative synchronization of the serial clock for exchange of data between bus partners with different maximum clock rates, defining a bus transaction scheme with addressing, framing of bits into bytes, and byte acknowledgement by the receiver.

Base Protocol establishes an asymmetrical interconnect between host computer and peripheral devices. The host is the ACCESS.bus manager, and data communication is always between host and peripheral, never between two peripherals. While the I²C Protocol establishes mastership between the sender or receiver of a bus transaction, Base Protocol defines the format of an ACCESS.bus message envelope, which is an I²C bus transaction with additional semantics, including checksum reliability control. Base Protocol also defines a set of seven control and status message types used in the configuration process.

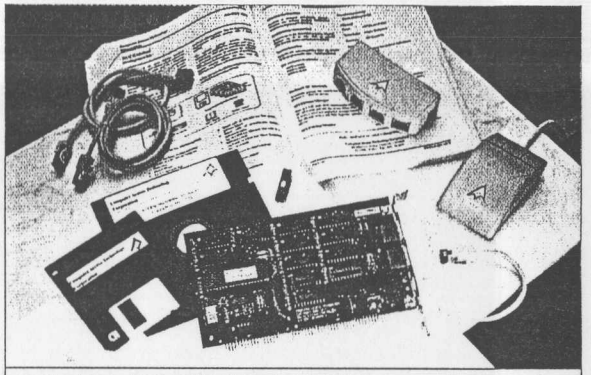


ACCESS.bus protocol hierarchy


ACCESS.bus connects keyboards, locators, and text-type devices to a system.

The high-level Application Protocol defines message semantics specific to particular functional types of devices. To date, Application Protocol have been established for keyboards, locators and text devices and is intended to define the simplest set of functions from common, industry-standard interfaces. Further, device-specific Application Protocol models will be defined by the ACCESS.bus Industry Group; and, of course, any vendor can implement a special device protocol within the general message envelope defined by the Base Protocol.

Electrically, host and peripheral devices are connected to serial data (SDA) and serial clock (SCL) lines in a wired-AND logic configuration, which can be implemented by connecting data and clock output stages of each bus partner to the SDA and SCL lines, respectively, through open-collector or open-drain transistors. Standard I²C components include these output stages on-chip. Significance of the wired-AND logic is that any attached bus partner can force either of these lines to LOW (GND); and when there is no output from any bus partner, lines are held HIGH by pull-up current sources in the host. Every bus partner can sense the level on both of these lines.


Called A.b-DEV-KIT, this ACCESS.bus product development support package from Computer Access Technology includes an IBM PC/AT-compatible Model A.b-1251 controller board, mouse, expansion box and cables, 87C751 µC, software, and user's manual. Price: $1500.

ACCESS.bus can be adapted to any platform and presently requires use of a controller board in the computer, but within 12 months, computer motherboards containing the necessary ACCESS.bus circuitry are expected to begin to appear. Software drivers are also available for DOS and Windows.

For additional information on ACCESS.bus v2.0 specs and on membership to ABIG, contact:

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